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Specification

1. [Title of the Invention]

IMAGE DISPLAY APPARATUS

2. [Scope of Claim]

(1) An image display apparatus for displaying, comprising:

a substrate having a pixel electrode connecting to an active element;

an opposed substrate; and

liquid crystal sandwiched between the substrate and the opposed substrate,

wherein a circuit for selecting a potential at a logical state determined by two inputs or three inputs for each electrode commonly connecting to active elements, thereby transmitting a signal to the electrode is integrated on the same substrate.

3. Detailed Description of the Invention

[Industrial Field for the Invention]

(1)

The present invention relates to an image display apparatus using liquid crystal sandwiched by a substrate forming a pixel electrode connecting to an active element and an opposed substrate.

[Prior Art]

(2)

In an active matrix image display apparatus for driving liquid crystal by active elements in each pixel electrode, each electrode commonly connecting to active elements is arranged as a lead electrode at an end side of a substrate. Signals are transmitted through a conductive rubber connector or a film flexible connector from off-substrate driver circuits.

[Problems to be Solved by the Invention]

(3)

In a high-density image display apparatus, a load of the connector connection is quite large. Accordingly, it is an object of the invention to provide an image display apparatus having an improved connection between the substrate and the off-substrate driver circuits.

[Means for Solving the Problem]

(4)

Accordingly, the present invention was made for preventing the addition of a new circuit from imposing a load on the production of a substrate by producing a circuit driving an electrode at a step of forming a substrate included in an image display apparatus and reducing the number of connection terminals with off-substrate driver circuits. According to the invention, an image display apparatus is provided for displaying by using liquid crystal sandwiched by a substrate forming a pixel electrode connecting to an active element and an opposed substrate. The apparatus is characterized in that a potential is selected at a logical state determined by two inputs or three inputs for each electrode commonly connecting to active

elements, and circuits transmitting signals to the electrode are integrated on one substrate.

(5)

FIG. 1 is a plan view of a liquid crystal display of an image display apparatus of the invention. (1) refers to a substrate having multiple pixel electrodes (3) connecting to active elements. (2) refers to an opposed substrate having common electrodes on the entire surface or on a surface of a side overlapping with the pixel electrodes (3) with reference to a chain line A-A'. The common electrodes are connected to an electrode (6) on (1) through conductive resin. (4) refers to a source electrode of the active element, that is a transistor, connected to (3). (5) refers to the gate electrode. The source electrodes are orthogonal to the gate electrodes, and the source electrodes and the gate electrodes are arranged in a matrix form. A pixel electrode connecting to an active element is positioned at each matrix point. (7) refers to an electrode provided for each pixel and commonly connecting to one electrode of a storage capacitor for pixel data. The electrodes (7) are arranged in series though they are shown by dashed lines instead. (9) refers to a driver circuit for gate electrodes commonly connecting to active elements. (9) is integrated on the substrate (1) at a step of forming active elements and pixel electrodes on the substrate (1). Electrodes for signals and power input to the driver circuit (9) are arranged as indicated by (8). Liquid crystal is sandwiched by the substrates (1) and (2).

(6)

FIG. 2 is a configuration diagram of a pixel of the image display apparatus of the invention, which is driven by an active element provided for each pixel. An active element (10) is a transistor. (11) refers to a storage capacitor for pixel data. (12) refers to a pixel electrode. (13) refers to a common electrode on a substrate opposed to (12). (14) refers to liquid crystal. (15) refers to a source electrode. (16) refers to a gate electrode. (10), (11), (12), (15) and (16) are provided on the substrate (1) in FIG. 1. (13) is provided on the substrate (2). A potential V_C of (13) is supplied from the electrode (8). A potential V_I of one electrode of (11) is supplied from the electrode (7). The transistor powered on by a gate signal applied to (16) transmits a source signal of (15) to the pixel electrode. Voltage between the pixel electrode and the common electrode is stored in the parallel capacitors (11) and (14). At the OFF state, an image is displayed by using the stored pixel data. The liquid crystal is alternately driven with reference to the common electrode potential by periodically changing the polarity of pixel data.

(7)

FIG. 3 is a diagram of driver circuits for gate electrodes commonly connecting to active elements of the image display apparatus of the invention. At a logical state determined by two inputs T_R (where R=1, 2 to K) and Q_S (where S=1, 2 to L) for each gate electrode, either a potential V_{SS} or a potential V_{DD} is selected, and a signal $P_{R,S}$ is transmitted to a $\{(R-1)\cdot L+S\}^{th}$ row. T_R, Q_S, V_{SS} and V_{DD} are signals and power input from the electrodes (8) shown in FIG. 1. By determining potentials of the gate electrodes at the K·L rows based on (K+L) input signals, the number of connection terminals with a driver circuit outside of the substrate is reduced like (8). The driver circuit for a signal $P_{1,1}$ includes a transistor (17) connecting T_1 to the drain through the capacitor (18) and having Q_1 as a gate input. A drain output of (17) is impedance-converted and is retrieved by a serial connection of a transistor (19) having Q_1 as a gate input and a transistor (20) having a drain output of the transistor (17) as a gate input. The source potentials of (17) and (19) are V_{SS} while the drain potential of (20) is V_{DD}. The drain of (19) and the source of (20) are connected. (21) refers to a capacitor attached to a first gate electrode. When both of (19) and (20) are OFF, the potential $P_{1,1}$ is maintained. In the configuration shown in FIGS. 1 and 2, this capacitor is a capacitor for an insulating film, for example, which is provided at the intersection of the gate electrode, the source electrode and the one electrode of the storage capacitor, a capacitor for liquid crystal sandwiched between the gate electrode and the common electrode on the opposed substrate and capacitors provided between the gate electrodes and V_{SS} and V_{DD} as required. The potentials V_{SS} and V_{DD} of the one electrode of the capacitors having the source electrode potentials V_I and V_C are collectively referred by V_{CC}. It is assumed here that a driver circuit for the gate electrode commonly connecting to active elements in figures excluding FIG. 3 naturally has a capacitor. Therefore, the capacitor is omitted in the figures.

[Operation]

(8)

FIG. 4 is a timing chart showing an operation of the driver circuit in FIG. 3. In following description, a potential relationship will be described based on an N-channel transistor. However, a potential relationship based on a P-channel transistor can be described similarly by reversing the potential relationship, for example.

(9)

T_R (where R=1, 2 to K) refers to a signal of a potential of V_{EE} to V_{GG}. L serial clock pulses from {(R-1)·L+1}th clock pulse from the clock pulse of the first V_{GG} (HIGH) of T_1 are output. Q_S (where S=1, 2 to L) refers to a signal of a potential of the V_{EE} to V_{GG}. Pulses of opposite phase V_{EE} (LOW) of Q_1 to Q_L are output one by one in synchronization with L clock pulses of T_R. $P_{R,S}$ is V_{DD} (HIGH) when T_R is V_{GG} (HIGH) and Q_S is V_{EE} (LOW). $P_{R,S}$ is V_{SS} (LOW) when Q_S is V_{GG} (HIGH). $P_{R,S}$ holds a previous state when T_R is V_{EE} (LOW) and Q_S is V_{EE} (LOW). Gate electrode signals $P_{1,1}$ to $P_{K,L}$ are sequentially output. When $P_{R,S}$ is V_{DD} (HIGH), Q_S is V_{EE} (LOW) and T_R is V_{EE} (LOW). Then, Q_S is V_{EE} (LOW) and T_R is V_{GG} (HIGH) (where $V_{DD}<V_{GG}$). Thus, the AND of the invert signal of Q_S and T_R is at HIGH. The potential of a point connecting to (17) of (18) at $P_{1,1}$ in FIG. 3 becomes HIGH, and V_{DD} is transmitted to the gate electrode through (20). (18) is constructed sufficiently larger than the capacitors excluding (18) connecting to the point. The potential at HIGH is substantially V_{GG}-V_{EE}+V_{SS}. In the driver circuit in FIG. 3, the source potential of (17) may be V_{EE} while the source potential of (19) may be V_{SS} (where $V_{EE} \leq V_{SS}$).

(10)

FIG. 5 is a substrate section diagram showing that a driver circuit for the gate electrode commonly connecting to active elements of the image display apparatus of the invention is integrated on a substrate having a pixel electrode connecting to an active element. (22) refers to the same glass substrate as (1) in FIG. 1. (23) refers to the gate of the transistor (17) in FIG. 3. (24) refers to one electrode to which a signal T_1 of the capacitor (18) is transmitted. (25) refers to an electrode connecting to the gate of the transistor (20) and a layer of Ni, Cr, Mo, Ta or the like. (26) refers to a gate insulating film of (17), (19) and (20) and a layer of SiO_2, Si_3N_4, Al_2O_3, Ta_2O_5 or the like, which is a dielectric of (18). (28) refers to a semiconductor layer of Si, Te, CdSe or the like of (17). (29) refers to a source electrode connecting to V_{SS} of (17). (30) refers to the drain of (17), one electrode of (18) and a layer of Al, Ni or the like connecting to (25) at a contact (27) of (26). (31) refers to a polyimide film and can have a laminated structure with a film having the same material as that of (26). A pixel has a pixel electrode having In_2O_3 and SnO_2 (ITO) layers connecting to the transistor (10) and the drain in FIG. 2 having the same layers as the layers (23), (26), (28), (29) and (30). The transistor includes a light-shielded film

on a semiconductor layer. The same film on the pixel electrode as the polyimide film of (31) is an orientation-processed layer resulting from rubbing. Rubbing is performed on the entire surface of the substrate (1) in FIG. 1 or one surface of the side having the pixel electrode (3) from the line A-A'. Rubbing may not be performed on the side having the driver circuit (9) of the electrode commonly connecting to the active elements with reference to the line A-A'. Similarly, when a seal for sealing liquid crystal is formed on the side, with reference to the line A-A', being larger than the area having the pixel electrode, excluding the driver circuit (9) and having the pixel electrode, liquid crystal is limited in the area having the pixel electrode. In FIG. 1, leads of gate electrodes to which signals from (9) are transmitted are disposed at the end side of the substrate (1). Therefore, each gate signal can be recognized even after a liquid crystal display is formed. However, in order to prevent the circuit (9) shown in FIG. 1 from functioning in accordance with an operational state, the inputs of (8) may be collectively connected to V_{SS} or V_{DD}. Alternatively, when liquid crystal is filled in an area having a pixel electrode like the above-described one, the liquid crystal display may be separated at the line A-A'. Then, like signals to the horizontally disposed source electrodes, signals are input thereto from the driver circuit outside of the substrate by using a connector connection from the gate electrode on the right side of the substrate. In the driver circuit for an electrode commonly connecting the active elements shown in FIG. 5, one surface on the left side with respect to the line A-A' of a glass surface of the substrate (22), that is the substrates (1) and (2) in FIG. 1, is coated. In this case, by sticking up an opaque sheet on the glass surface or placing the glass surface within a case, the glass surface is shielded from light. A liquid crystal display having a polarizer has an off-substrate driver circuit and is disposed within a case. Thus, a reflective or light-transmissive image display apparatus is obtained with a reflector or light source on the back of the substrate.

(11)

The description above relates to the improvement of an image display apparatus transmitting signals from an off-substrate driver circuit through a connector at an end side of the substrate of a liquid crystal display. The invention may be applied to the improvement of an image display apparatus having, in a chip form or in a package on a substrate of a liquid crystal display, a driver circuit for electrodes commonly connecting to active elements, such as an

integrated circuit including a shift register driving gate electrodes, a shift register driving source electrodes and a latch. FIG. 6 is a plan view of a liquid crystal display of the image display apparatus of the invention like FIG. 1. (32), (33), (34), (35), (36), (37), (38), (39) and (40) correspond to (1), (2), (3), (4), (5), (6), (7), (8) and (9) respectively and are sandwiched between substrates (32) and (33). (51), (52), (53) and (54) refer to integrated circuits of shift registers and latches, which drive source electrodes. Signals input to the integrated circuits include clocks of the shift registers, data, write-enable signals for writing data to the latches, and polarity signals for inverting latch outputs. Six lead electrodes including two electrodes of a power source are disposed on the right side of the substrate. (41) refers to data. (42) refers to a clock. (43) refers to a write-enable signal. (44) and (45) refer to positive and negative electrodes of the power source. (38) refers to an electrode for generating a polarity signal of the latch at an input potential V_i in FIG. 2 of one electrode of a storage capacitor for pixel data. (38) may have the same input as that of the common electrode (37). (55) refers to an integrated circuit generating signals T_R (where R=1, 2 to K) and Q_S (where S=1, 2 to L) shown in FIG. 3 transmitted to a driver circuit (40) for electrodes commonly connecting active elements, that is, a gate electrode provided on one substrate at a step of producing the substrate (32) having pixel electrodes connecting to the active elements. Clocks that T_R and Q_S are based on and power source inputs V_{GG} and V_{EE} shown in FIG. 4 are input from the lead electrodes (46), (47) and (48) on the left side of the substrate to (55). (49) and (50) refer to negative and positive electrodes of the power sources V_{SS} and V_{DD} in FIG. 3. As shown in FIGS. 1 and 6, the total number of source electrodes is equal to the number of connection terminals between the source electrodes and the off-substrate driver circuits and the number of output terminals from the integrated circuit implemented on the substrate to the source electrodes. On the other hand, by integrating the driver circuit (40) for the gate electrodes on the same substrate, the number of connection terminals with the off-substrate driver circuits on the gate electrode side and the number of output terminals from the integrated circuit (55) implemented onto the substrate to (40) are significantly lower than the total number of gate electrodes. A line B-B' corresponds to the line A-A' in FIG. 1. The positions of the rubbing of the orientation-processed layer of the substrate (32) and of the sealing of the common electrode and liquid crystal of the opposed electrode are limited in the side having the pixel electrodes with respect to the B-D-D' rather than the side

having the integrated circuit. By dividing at lines B-B', C-C', B'-C"-C' or the like in accordance with a condition, signals can be input from the lead electrode at an end side of the substrate, as described above. Input signals and power to the driver circuit for the source electrodes and gate electrode are arranged on the upper side of the substrate while the gate electrodes have lead electrodes on the right side of the substrate. A dual-layer wire from the lead electrode at the end side of the substrate to the integrated circuit implemented on the substrate is formed on the substrate by using a material of the same layers as the (23), (24) and (25) and (29) and (30) shown in FIG. 5. The wired area is covered by the opposed substrate (33) like the driver circuit (40) for the gate electrode. An insulating film of the terminal part implemented on the integrated circuit is removed, and the terminal connection between the integrated circuit and the substrate is achieved by plating the terminals on the substrate as required, and resin-sealing by using wire-bonding or bonding through a face-down boundary flow for a chip product or performing soldering connection for a package product.

(12)

FIGS. 7 and 8 are diagrams of driver circuits for gate electrodes commonly connecting to active elements of the image display apparatus of the invention like FIG. 3. FIG. 9 is a timing chart showing an operation thereof. The potential of the V_{SS} or V_{DD} is selected based on a logical state determined by two inputs T_R and Q_S in FIG. 7 and T_R and Q'_S in FIG. 8 for each gate electrode. Signals $P_{R,S}$ are supplied to a $\{(R-1)\cdot L+S\}^{th}$ row. FIG. 7 includes a serial connection of transistors (56), (57) and (58) having ϕ, T_R and Q_S as respective gate inputs. When the source potential of (56) is VSS and the drain potential of (58) is V_{DD}, T_R and Q_S are both VGG (HIGH). In other words, when the AND is HIGH, (57) and (58) are turned on. Thus, $P_{R,S}$ are at V_{DD} (HIGH). When either one is at V_{EE} (LOW), a clock ϕ has the potential V_{SS} (LOW) to be pre-charged through (58) at V_{GG}. FIG. 8 includes a serial connection of transistors (59) and (60) having ϕ and T_R as respective gate inputs. When the source potential of (59) is V_{SS} and the drain potential of (60) is Q'_S, the T_R is at V_{GG} (HIGH) while Q_S is at V_{DD} (HIGH). In other words, when the AND is HIGH, (60) causes $P_{R,S}$ to have V_{DD} (HIGH). When T_R is at V_{EE} (LOW) or Q'_S is at V_{SS} (LOW), a clock ϕ has the potential V_{SS} (LOW) to be pre-charged through the (59) at V_{GG}. In substantially the same manner as that of the timing chart in FIG. 4, T_R refers to a signal at a potential of V_{EE} to V_{GG}. T_R outputs L serial clock

pulses from $\{(R-1)\cdot L+1\}^{th}$ clock pulse from the first clock pulse at HIGH of T_1. Q_S and Q'_S refer to signals at potentials of V_{EE} to V_{GG} and V_{SS} to V_{DD}. Pulses of same phase of Q_1 to Q_L and Q'_1 to Q'_L are output one by one in synchronization with L clock pulses T_R. Clocks ϕ common to driver circuits for gate electrodes are serial signals having V_{GG} (HIGH) when T_R and Q_S or Q'_S are both LOW, that is, V_{EE} or V_{SS} and having V_{EE} (LOW) when either one is HIGH, that is, V_{GG} or V_{DD}. Gate electrode signals $P_{R,1}$ to $P_{R,L}$ are sequentially output. The circuit shown in FIG. 8 can have Q_S as a gate input of (60) and a signal T'_R at a potential of V_{SS} to V_{DD} in the same phase as T_R as the drain potential. In this case, T'_R is at V_{DD} (HIGH) while Q_S is at V_{GG} (HIGH). Thus, when the AND is HIGH, $P_{R,S}$ is at V_{DD} (HIGH). When T'_R is at V_{SS} (LOW), the clock ϕ has the potential V_{SS} (LOW) to be pre-charged through the (59) at V_{GG} independently from the logical state of Q_S.

(13)

FIG. 10 shows a construction in which V_{SS} in FIG. 8 is replaced by Q'_S. (59) and (60) correspond to (61) and (62) respectively. FIG. 10 includes a parallel connection of transistors (61) and (62) having ϕ and T_R as respective gate inputs. The source potential is Q'_S, and the drain is an output $P_{R,S}$. When T_R is at V_{GG} (HIGH) and Q'_S is at V_{DD} (HIGH), (62) causes $P_{R,S}$ to have V_{DD} (HIGH). When T_R is V_{EE} (LOW) and Q'_S is V_{SS} (LOW), a clock ϕ has the potential of Q'_S (LOW) to be pre-charged through (61) at V_{GG}. Signals are defined such that Q'_S can be always at V_{SS} (LOW) when ϕ is at V_{GG}. Clocks ϕ are common to the driver circuits for the gate electrodes. The same function can be achieved in the circuits in FIGS. 8 and 10 when the sources (59) and (61) are T_R, and the LOW potential V_{EE} of T_R is V_{SS}. In this case, signals are also defined such that T_R can be always at V_{SS} (LOW) when ϕ is at V_{GG}. In the circuit in FIG. 10, like the circuit in FIG. 8, the gate input of (62) can be a signal Q_S at a potential of V_{EE} to V_{GG}. The source potentials of (61) and (62) can be a signal T'_R at a potential of V_{SS} to V_{DD} of the same phase as that of T_R. When Q_S is at V_{GG} (HIGH) and T'_R is at V_{DD} (HIGH), $P_{R,S}$ is at V_{DD} (HIGH). When Q_S is at V_{EE} (LOW) and T'_R is at V_{SS} (LOW), the clock ϕ has a potential T'_R (LOW) to be pre-charged through (61) at V_{GG}. Signals are defined such that T'_R can be always at V_{SS} (LOW) when ϕ is at V_{GG}.

(14)

FIG. 11 includes a construction in which power sources V_{SS} and V_{DD} (where $V_{SS}<V_{DD}$)

in FIG. 7 are exchanged. (63), (64) and (65) correspond to (56), (57) and (58) respectively. When T_R and Q_S are both at V_{GG} (HIGH), $P'_{R,S}$ is at V_{SS} (LOW). When either one is at V_{EE} (LOW), a clock ϕ has the potential (HIGH) of V_{DD} to be pre-charged through (63) at V_{GG}. Thus, signals of opposite phase to those of $P_{R,1}$ to $P_{R,L}$ in FIG. 9 are output. In FIG. 8, V_{SS} is replaced by V_{DD}, and an invert signal of Q'_S at a potential of V_{SS} to V_{DD} is obtained instead of Q'_S. The same output as that in FIG. 11 can be obtained by replacing Q'_S by the invert signal of Q'_S in FIG. 8, for example. ϕ, T_R, Q_S and the invert signal of Q'_S in these circuits may be slightly delayed from ϕ, T_R, Q_S and Q'_S in FIGS. 7, 8 and 10. Alternatively, a leading edge from V_{EE} to V_{GG} of ϕ or a leading edge from V_{SS} to V_{DD} of the invert signal of Q'_S may be delayed from a falling edge from V_{GG} to V_{EE} of T_R. The output may be used as a compensating signal disclosed in JP-A-56-195295, "GAZOU HYOJI SOCHI (IMAGE DISPLAY APPARATUS)".

(15)

FIG. 12 is diagrams of driver circuits for electrodes commonly connecting to active elements of the image display apparatus of the invention, which are obtained when a compensating signal electrode of pixels in a row as disclosed in the application also functions as an electrode commonly connecting active elements at an adjacent row thereto. FIG. 13 is a timing chart showing an operation thereof. FIG. 12 shows a circuit outputting signals $P_{R,1}$ and $P_{R,2}$ for driving gate electrodes at $\{(R-1)\cdot L+1\}^{th}$ and $\{(R-1)\cdot L+2\}^{th}$ rows. The circuit outputting $P_{R,1}$ is constructed by connecting a serial connection of transistors (67) and (68) having T_R and Q_1 as respective gate inputs, a serial connection of transistors (69) and (70) having T_R and Q_2 as respective gate inputs and the transistor (66) to the output terminal. The source potential of (66) is at V_{SS}. The drain potential of (68) is at V_{DD}. The source potential of (70) is V_{GG}, and $V_{GG}<V_{SS}$. The circuit outputting $P_{R,2}$ is constructed by connecting a serial connection of transistors (72), (73) having T_R and Q_2 as respective gate inputs, a serial connection of transistors (74) and (75) having T_R and Q_3 as respective gate inputs and a transistor (71) having $\phi 2$ as a gate input to the output terminal. The source potential of (71) is V_{SS}. The drain potential of (73) is V_{DD}. The source potential of (75) is V_{BB}. The circuits (69) and (70) outputting $P_{R,1}$ and the circuits (72) and (73) at the next row outputting $P_{R,2}$ have a same gate input signal. (69) and (70) having V_{BB} as the source potential compensate an influence of a change in gate potential on a potential of the pixel electrode when (72) and (73) having V_{DD} as the drain potential are

switched from ON to OFF. Similarly, the circuits (74) and (75) outputting $P_{R,2}$ generate a compensating signal of pixels at the next row. $\phi 1$ and $\phi 2$ are clocks at potentials V_{EE} to V_{GG} (where $V_{EE} \leq V_{BB}$) common to driver circuits of gate electrodes at odd-numbered rows and even-numbered rows, respectively. T_R refers to a signal at a potential of V_{EE} to V_{GG}. L serial clock pulses from $\{(R-1)\cdot L+1\}^{th}$ clock pulse from the first clock at HIGH of the T_1 are output. Q_S (where S=1, 2, 3 to L) refers to a signal at a potential of V_{EE} to V_{GG}. Pulses of same phase of Q_1, Q_2, Q_3 to Q_L are output one by one in synchronization with L clock pulses T_R. $\phi 1$ and $\phi 2$ are serial signals to be at V_{GG} (HIGH) when T_R and Q_S are both LOW, that is, V_{EE}, and to be at V_{EE} (LOW) when either one is HIGH, that is, V_{GG}. The serial signals $\phi 1$ and $\phi 2$ have a delayed leading edge from V_{EE} to V_{GG} alternately. When delayed, a leading edge turning off the transistor having T_R and Q_S as gate inputs and V_{BB} as the source potential and changing the output $P_{R,(S-1)}$ or $P_{(R-1),1}$ from V_{BB} to V_{SS} is delayed from a falling edge turning off the transistor having T_R and Q_S at the next row as gate inputs and V_{DD} as the drain potential and changing the output $P_{R,S}$ from V_{DD} to V_{SS}. Thus, an influence from a change in gate potential of pixel electrodes connecting to transistors having $P_{R,S}$ as a common gate input can be compensated. As indicated by the outputs $P_{R,1}$ and $P_{R,2}$, pulse signals having a potential changed from V_{DD} to V_{BB} are sequentially output. The signal varying from V_{BB} to V_{SS} is a compensating signal for pixel electrodes connecting to a transistor to be turned on or off by a signal varying from V_{DD} to V_{SS}. When a compensating capacitor C_X for a pixel electrode is disposed so as to achieve real N times of the capacitance between the gate and the drain of the transistor, V_{BB} is selected as a potential of $(V_{SS}-V_{DD})/N+V_{SS}$.

(16)

In the timing charts in FIGS. 9 and 13, Q_S and Q'_S are synchronized with clock pulses of T_R at HIGH. However, the pulse width may be wider than the shown width and, for example, may be equal to one cycle having a pair of clocks at HIGH and LOW among L serial clock pulses of T_R. In this case, ϕ, $\phi 1$ and $\phi 2$ may be serial clocks, which are at HIGH when clock pulses of T_R are at LOW. Alternatively, pulses at HIGH of L serial clock pulses of T_R may be changed to pulses at LOW or the pulse width may be larger than that of Q_S or Q'_S. In this case, ϕ, $\phi 1$ and $\phi 2$ may be serial clocks at HIGH when Q_1 to Q_L and Q'_1 to Q'_L have LOW at the same time. Thus, the circuits in FIGS. 7, 8, 10, 11 and 12 can be operated.

(17)

In the above-described driver circuit for electrodes commonly connecting to the active elements, a transistor having the invert signal of Q_S, ϕ, $\phi 1$ and $\phi 2$ as gate inputs, having the output of $P_{R,S}$ at HIGH when the AND of T_R and the invert signal of Q_S, Q_S and Q'_S is at HIGH and at HIGH when the AND of T_R and the invert signal of Q_S, Q_S or Q'_S is at LOW statically causes the output of $P_{R,S}$ at LOW. Thus, when the potential of the source electrode of a liquid crystal display is determined in the LOW period, the potential of the source electrode does not affect the potential of the gate electrode through the overlapping capacitor. On the other hand, a liquid crystal display is constructed such that a capacitance between the gate electrode and the source electrode can be sufficiently small in a capacitance attached to the gate electrode. For example, a connection between the source electrode and gate electrode of a transistor connecting to a pixel electrode has a self-alignment structure. In a structure where an electrode, such as a one-side electrode, at a fixed potential of a storage capacitor for pixel data is provided at an intersection between the source electrode and the gate electrode, which are arranged in a matrix form, a capacitor attached to the gate electrode may be a capacitor of an insulating film sandwiched with the electrode at the fixed potential or a liquid crystal capacitor sandwiched with a common electrode of an opposed substrate. The potential of the gate electrode for turning off the transistor connecting to the pixel electrode is dynamically held while the potential of the source electrode is changed.

(18)

In FIG. 14, the transistor (76) having Q_S at a potential of V_{EE} to V_{GG} as the gate input and having T'_R at V_{SS} to V_{DD} as the source potential transmits signals to a commonly connected gate electrode by using $P_{R,S}$ as the drain output. T'_R outputs L serial clock pulses from the $\{(R-1)\cdot L+1\}^{th}$ clock pulse from the first clock pulse at V_{DD} (HIGH) of T_1'. Q_S outputs pulses Q_1 to Q_L one by one in synchronization with the L clock pulses from T'_R. The pulse width is substantially the same as a cycle of one pair of clocks at HIGH and LOW in the L serial clock pulses of the T'_R. As shown in a timing chart in FIG. 15, the synchronized Q_S and T'_R has a relationship that, when Q_S is at V_{GG} (HIGH), the clock pulses from T'_R have two states of V_{DD} (HIGH) and V_{SS} (LOW). When T'_R is at HIGH and Q_S is at HIGH, that is, the AND is at HIGH, $P_{R,S}$ is at V_{DD} (HIGH). Then, when T'_R is at LOW and Q_S is at HIGH, the $P_{R,S}$ is at V_{SS} (LOW).

After that, $P_{R,S}$ dynamically holds the potential at LOW when Q_S is at HIGH and until the potential of Q_S with T'_R at LOW is led to $P_{R,S}$. As indicated by $P_{R,1}$ to $P_{R,L}$, $P_{R,S}$ sequentially outputs signals for turning on transistors commonly connecting to each gate electrode. A period for dynamically holding the potential at LOW is a frame cycle/K of the image display apparatus.

(19)

When a potential of one electrode of a storage capacitor for pixel data and a potential of a common electrode on an opposed substrate are fixed, and when liquid crystal is alternately driven by changing a potential to be applied to the source electrode, a potential at V_{SS} (LOW) of each gate electrode may be adjusted by a frame so as to be equal to or lower than the source potential or may be continuously maintained as a fixed potential. In order to adjust the potential by a frame by dynamically holding the potential at LOW of each gate electrode at the same time, a period may be prepared in FIGS. 14 and 15 in which both of the potentials of T'_1 to T'_R are LOW, which is required to change, and Q_1 to Q_L lead LOW potentials to the gate electrodes. In order to alternately drive liquid crystal by changing the potential of the one electrode of the storage capacitor for pixel data and the potential of the common electrode of the opposed substrate, a potential at V_{SS} (LOW) of each gate electrode may be adjusted by a frame as described above so as to be equal to or lower than the potential of the pixel electrode depending on these changes in potentials and the source potential or may be continuously fixed. When the potential at LOW of each gate electrode is dynamically held, and since the potential at LOW depends on changes in potential of the one electrode of the storage capacitor and potential of the common electrode, the fixed potential of V_{SS} may be determined for T'_1 to T'_K in advance so as to be equal to or lower than the potential of the pixel electrode and the source potential even after the changes. Alternatively, as described above, a period may be prepared in which the potentials of T'_1 to T'_K are potentials at LOW, which is required to change and Q_1 to Q_L lead potentials at LOW to the gate electrodes. Thus, the potential at LOW of the gate electrodes can be adjusted by the frame. The potential of V_{SS} may be adjusted by maintaining a constant voltage in V_{DD} and V_{SS} or a constant voltage in V_{GG}-V_{DD}-V_{SS}-V_{EE} at the same time.

(20)

FIG. 16 shows driver circuits. In the timing chart in FIG. 9, $P_{R,1}$ to $P_{R,L}$ are sequentially output for each cycle of one pair of clocks at HIGH and LOW among L serial clock pulses of T_R.

The pulse width is the pulse width of a clock at HIGH. On the other hand, the driver circuits change the state to a state that, as shown in a timing chart in FIG. 17, $P_{R1,1}$ and $P_{R2,1}$ to $P_{R1,L}$ and $P_{R2,L}$ are sequentially output for each half cycle of a pair of clocks at HIGH and LOW among L serial clock pulses and the pulse width is the half cycle. The driver circuits output signals $P_{R1,S}$ and $P_{R2,S}$ to odd-numbered and even-numbered gate electrodes adjacent to the $\{(R_1-1)\cdot 2L+2S-1\}^{th}$ and $\{(R_2-2)\cdot 2L+2S\}^{th}$ (where R2=R1+1) gate electrodes. The circuit outputting $P_{R1,S}$ includes a serial connection of transistors (77), (78) and (79) having $\phi 1$, $T_{R,L}$ and Q_S as the respective gate inputs. The source potential of (77) is V_{SS} while the drain potential of (79) is V_{DD}. The circuit outputting $P_{R2,S}$ includes a serial connection of transistors (80), (81) and (82) having $\phi 2$, T_{R2} and Q_S as the respective gate inputs. The source potential of (80) is V_{SS} while the drain potential of (82) is V_{DD}. When all of Q_S, T_{R1} and T_{R2} have V_{GG} (HIGH), that is, the AND is at HIGH, the outputs $P_{R1,S}$ and $P_{R2,S}$ have V_{DD} (HIGH). When T_{R1} and T_{R2} have V_{EE} (LOW), the outputs are V_{GG}. Thus, a transistor having the clocks $\phi 1$ and $\phi 2$ causing these states can have a potential at V_{SS} (LOW) to be pre-charged. T_{R1} and T_{R2} continuously output L clock pulses at HIGH alternately from the $\{(R1-1)\cdot 2L+1\}^{th}$ clock pulse from the first clock at HIGH of T_{1L} among signals at potentials of V_{EE} to V_{GG}. Q_S sequentially outputs pulses at HIGH having a width equal to a sum of widths of the S^{th} clock pulses at HIGH from the first clock pulses at HIGH from T_{R1} and T_{R2} among signals at potentials of V_{EE} to V_{GG}. $\phi 1$ and $\phi 2$ are serial signals resulting from the inversion of L serial clocks of T_{R1} and T_{R2} among signals at potentials of V_{EE} to V_{GG} common to the driver circuits for gate electrodes at the odd-numbered and even-numbered rows. $P_{R1,S}$ and $P_{R2,2}$ are statically fixed at LOW when $\phi 1$ and $\phi 2$ have V_{GG} (HIGH). $P_{R1,S}$ and $P_{R2,2}$ are dynamically fixed at LOW when $\phi 1$ and $\phi 2$ have V_{EE} (LOW) except when the AND of T_{R1} and T_{R2} and Q_S is at HIGH. In the circuits in FIG. 16, the drain potentials of (78) and (81) may be Q'_S of same phase as Q_S and have a potential of V_{SS} to V_{DD} and (79) and (82) may be removed, as shown in FIG. 8. Furthermore, a driver circuit may be provided. In this case, clock pulses at HIGH of T_{R1}, T_{R2} to T_{RN} are sequentially output in HIGH periods of Q_S. Q_1, Q_2 to Q_L have HIGH in accordance with the sequential outputs of L or fewer serial clock pulses from T_{R2} to T_{RN}. $\phi 1$, $\phi 2$ to ϕN are invert signals of T_{R1}, T_{R2} to T_{RN}. The driver circuit outputs $P_{R1,S}$, $P_{R2,S}$ to $P_{RN,S}$ (where S=1 to L) as shown in FIG. 16. The driver circuit may be adjusted to sequentially output signals $P_{R1,1}$, $P_{R2,1}$ to $P_{RN,1}$ to $P_{R1,L}$, $P_{R2,L}$ to $P_{RN,L}$ as

shown in FIG. 17. In this case, serial gate signals at N rows are output until the N·L rows in a same sequence and are output until the K·N·L rows where R=1 to K. Q_S is L input signals, and T_{11} to T_{KN} are K·N input signals. $\phi 1$ to ϕN are clock signals common to K·L gate electrodes and are used for pre-charging.

[Embodiments]

(21)

FIG. 18 is a plan view of a liquid crystal display of an image display apparatus according to an embodiment of the invention. (83) refers to a substrate having multiple pixel electrodes (85) connecting to active elements. (84) refers to an opposed substrate having multiple column electrodes overlapping with the pixel electrodes. (86) forms a storage capacitor for pixel data with each pixel electrode in one column including (85). (87) on the substrate (83) refers to a column electrode which overlaps with each pixel electrode in one column on the substrate (84). (88) and (89) refer to two row electrodes which are used in pairs in the pixels in one row including (85). An active element and a pair of diodes are connected between each pixel electrode and two row electrodes, and the pair of the row electrodes are connected to the right and left sides respectively so that signals are transmitted to each of the electrodes from driver circuits (92) and (93) for row electrodes on the substrate (83). (92) and (93) are integrated at a step of producing the active elements, the column electrodes and the pixel electrodes on the substrate. Signals input to (92) and (93) are arranged on the upper side of the substrate as well as the column electrodes as shown in (90) and (91). Thus, the number of lead electrodes for the signals is much smaller than the total number of the row electrodes. Liquid crystal is sandwiched between the substrates (83) and (84), and the positions of the rubbing of an orientation-processed layer of the substrate (83) and of a seal for sealing the liquid crystal may be limited in the side having the pixel electrodes surrounded by lines E-E' and F-F' excluding the driver circuits for row electrodes on the substrate as shown in FIG. 1 with respect to the line A-A'.

(22)

FIG. 19 is a configuration diagram of a pixel of the image display apparatus according to an embodiment of the invention. (94) and (95) are a pair of diodes each arranged in the reverse direction. (96) refers to a pixel electrode. (97) refers to a storage capacitor for pixel

data. (98) refers to a column electrode, that is one electrode of (97) for forming a storage capacitor with each pixel electrode. (99) refers to a column electrode on the opposed substrate to (96), and the same signal is applied to (98) and (99). (100) refers to liquid crystal. (101) and (102) refer to two row electrodes which are used in pairs and have diodes each arranged in the reverse direction between (96). (94), (95), (96), (97), (98), (101), and (102) are formed on the substrate (83) in FIG. 18, and (99) is formed on the substrate (84). In the selection period of pixels in one row, row signals transmitted from the driver circuits (92) and (93) to the row electrodes (101) and (102) are led to the pixel electrode through the diodes, and a voltage difference between data applied to each column electrode (98) and (99) is stored as pixel data in the parallel capacitors (97) and (100). In the non-selection period, potentials of the row electrodes which are opposed to the pixel electrode are fixed so that the pair of the diodes are biased in the reverse direction in order to hold the voltage stored in the selection period, and thus to display an image. Liquid crystal is alternately driven by periodically changing the polarity of pixel data.

(23)

FIG. 20 shows diagrams of driver circuits for gate electrodes commonly connecting to active elements of the image display apparatus according to an embodiment of the invention. FIG. 21 is a timing chart showing an operation thereof. FIG. 20 shows driver circuits for two row electrodes which are used in pairs in the pixels at a $\{(R-1)\cdot L+S\}^{th}$ row. $P_{R,S}$ and $P'_{R,S}$ are output to (101) and (102) respectively. At a logical state determined by two inputs of T_R and Q_S, or T'_R and Q'_S, either one of a potential V_{DD}, V_{SS}, or a potential in the vicinity of V_{SS} is selected, and either one of a potential V_{DD}, V_{HH}, or a potential in the vicinity of V_{HH} is selected to be transmitted to each row electrode. In the circuit outputting $P_{R,S}$, an N-type semiconductor layer of a diode (103) is connected to T_R while a P-type semiconductor layer thereof is connected to Q_S through a resistor (104). Meanwhile in the circuit outputting $P'_{R,S}$, a P-type semiconductor layer of a diode (105) is connected to T'_R while an N-type semiconductor layer thereof is connected to Q'_S through a resistor (106). In substantially the same manner as that of the timing chart in FIG. 4, T_R refers to a signal at a potential of V_{SS} to V_{DD} ($V_{SS}<V_{DD}$). L serial clock pulses from $\{(R-1)\cdot L+1\}^{th}$ clock pulse from the first clock pulse at HIGH of T_1 are output. Q_S refers to a signal at a potential of V_{SS} to V_{DD}. Pulses of same phase of Q_1 to Q_L are output one

by one in synchronization with the L clock pulses of T_R. T'_R and Q'_S refer to signals at potentials of V_{DD} to V_{HH} ($V_{DD}<V_{HH}$) and each have opposite phase to those of T_R and Q_S. In the circuit outputting $P_{R,S}$, when each of T_R and Q_S is at V_{DD} (HIGH), that is, the AND is at HIGH, the output $P_{R,S}$ is at V_{DD} (HIGH), and when either one of T_R and Q_S is at V_{SS} (LOW), the output has a potential in the vicinity of V_{SS} or V_{SS} (LOW). In the circuit outputting $P'_{R,S}$, when each of T'_R and Q'_S is at V_{SS} (LOW), that is, the OR is at LOW, the output $P'_{R,S}$ is at V_{DD} (LOW), and when either one of T'_R and Q'_S is at V_{HH} (HIGH), the output has a potential in the vicinity of V_{HH} or V_{HH} (HIGH). The term vicinity herein refers to a potential of Q_S which is led by the capacitor (104) after the diode (103) is biased in the reverse direction in the case where the potential of T_R is higher than that of Q_S. Meanwhile in the case where the potential of T_R is lower than that of Q_S, the term vicinity refers to the potential in which a voltage for the diode in the forward direction is added to T_R, that is a potential in the vicinity of T_R. As shown in $P_{R,1}$ to $P_{R,L}$, row signals are sequentially output. $P'_{R,1}$ to $P'_{R,L}$ are synchronized signals having the opposite phase. V_{HH} is determined by $2V_{DD}-V_{SS}$. T_R and Q_S in FIG. 20 may be exchanged as well as T'_R and Q'_S. Alternatively, a duty ratio of HIGH and LOW of clock pulses among L serial clock pulses of T_R and T'_R may be changed so as to operate the circuit with the widened clock pulse width of T_R at HIGH and T'_R at LOW. Alternatively, as shown in FIGS. 16 and 17, clock pulses at HIGH of T_{R1} and T_{R2} may be sequentially output in HIGH periods, and in accordance with the sequential outputs of L serial clock pulses which are alternately output from T_{R1} and T_{R2}, Q_1, Q_2 to Q_L may be fixed at HIGH and $P_{R1,1}$, $P_{R2,1}$ to $P_{R1,L}$ and $P_{R2,L}$ are output as well as the opposite phase of $P'_{R1,1}$, $P'_{R2,1}$ to $P'_{R1,L}$ and $P_{R2,L}$.

(24)

FIG. 22 is a substrate section diagram showing an embodiment that a driver circuit for row electrodes commonly connecting to active elements of the image display apparatus of the invention is integrated on a substrate having a pixel electrode connecting to an active element. (107) refers to the same glass substrate as (83) in FIG. 18. (108) refers to an electrode connecting to an N-type semiconductor layer of the diode (103) in FIG. 20 and a layer of Ni, Cr, Mo, Ta or the like. (109), (110) and (111) refer to N-type, I-type and P-type semiconductor layers of Si deposited by CVD respectively, which correspond to the diode (103). (112) refers to an insulating film of SiO_2, Si_3N_4, SiOxNy or the like. (115), (116) and (117) are layers of Al,

Ni or the like. (115) refers to a signal electrode of T_R connecting to (108) at a contact (113). (116) refers to an electrode connecting to the P-type semiconductor layer of (103) at a contact (114). (117) refers to a signal electrode of Q_S. (118) connecting to (116) and (117) corresponds to the resistor (104) formed of a layer of In_2O_3 SnO_2 (ITO). (119) refers to a polyimide film and can have a laminated structure with a film formed of the same material as that of (112). A pixel has the diodes (94) and (95) shown in FIG. 19 and a pixel electrode formed of the same layer as (18) connecting to the electrode of the diodes. A film on the same layer as the polyimide film of (119) on the pixel electrode is to be an orientation-processed layer resulting from rubbing.

(25)

As active elements and diodes according to an embodiment of the invention, as well as the above-described PIN junction diode, a MIN Schottky diode in which a P-type semiconductor layer of the PIN structure is replaced by a metal can be used. In that case, the row electrodes connecting to the driver circuits (92) and (93) of the liquid crystal display shown in FIG. 18 may be arranged on the side having the driver circuits with respect to lines E-E' and F-F', and formed to have the similar shapes and structures of the lead electrodes of the row electrodes at the end side of the substrate. The substrate can be cut off on the side having the driver circuits as needed with respect to the lines E-E' and F-F', taking the lead electrodes of the row electrodes as the end side of the substrate. Thus, a liquid crystal display can be constructed by overlapping the cut-off substrate with its conformable opposed substrate, in which the driver circuits for row electrodes arranged on the right and left side of the substrate are integrated into one side.

(26)

FIG. 23 is a plan view of a liquid crystal display of the image display apparatus according to an embodiment of the invention. (120) refers to a substrate having multiple pixel electrodes (122) connecting to active elements. (121) refers to an opposed substrate having common electrodes on the entire surface or on a surface of a side overlapping with the pixel electrodes (122) with reference to a chain line G'-H"-H'. The common electrodes are connected to an electrode of (125) on (120) through conductive resin. (123) refers to a source electrode of the active element, that is a transistor, connected to (122). (124) refers to a gate electrode thereof. The source electrodes are orthogonal to the gate electrodes, and they are arranged in a

matrix form. A pixel electrode connecting to an active element is positioned at each matrix point. (126) refers to an electrode commonly connecting to one electrode of a storage capacitor for pixel data which is formed in each pixel as shown by dashed lines. (128) refers to a driver circuit for gate electrodes commonly connecting to active elements. (130) refers to a driver circuit for source electrodes commonly connecting to active elements. (130) is integrated on the substrate (120) at a step of forming active elements and pixel electrodes on the substrate (120). Electrodes for signals and power input to (128) and (130) are arranged at the end side of the substrate as indicated by (127) and (129), and the number of the electrodes is much smaller than the total number of the gate electrodes and the source electrodes. Liquid crystal is sandwiched between the substrates (120) and (121), and the positions of the rubbing of an orientation-processed layer of the substrate (120) and of the sealing of for the liquid crystal is limited in the side having the pixel electrodes surrounded by a line G'-H"-H' excluding the driver circuits (128) and (130). Depending on the circumstances, the substrate is cut off with respect to lines G-G' and H-H' or the like to construct a liquid crystal display overlapping the substrate with its conformable opposed substrate, in which signals are supplied to each lead electrode for the gate electrodes and the source electrodes at the end side of the substrate. The driver circuit for gate electrodes are constructed as in FIGS. 3, 7, 8, 10, 11, 12, 14 and 16. The driver circuit for gate electrodes and source electrodes are integrated on the substrate having a pixel electrode connecting to an active element as shown in FIG. 5.

(27)

FIG. 24 is a diagram showing another embodiment of a driver circuit for the source electrode commonly connecting to active elements of the image display apparatus of the invention. The potential of data D is selected based on a logical state determined by two inputs T_R (where R=1, 2 to K) and Q_S (where S=1, 2 to L) for each source electrode. A signal $O_{R,S}$ is supplied to a $\{(R-1)\cdot L+S\}^{th}$ row. Although the input signals of T_R, Q_S or the like are denoted by the same symbols as those of the driver circuit for the gate electrode for ease of description, they are distinctive signals for each of the driver circuits for the gate electrode and the source electrode. While the driver circuit for the gate electrode scans gate electrodes in one row at a logical state determined by T_R and Q_S, the driver circuit for the source electrode transmits data which is selected at the logical state determined by each of T_R and Q_S to the pixels in one row

through the source electrode. In the case of constructing the driver circuit for the gate electrode like FIGS. 3, 7, 8, 10, 11 and 12, the driver circuit for the source electrode selects data at a logical state determined by T_R and Q_S while a transistor having an invert signal of Q_S, ϕ, $\phi 1$ and $\phi 2$ at HIGH as gate inputs statically causes the output of $P_{R,S}$ to be at LOW. A liquid crystal display is constructed such that a capacitance between the gate electrode and the source electrode can be sufficiently small among capacitances attached to the gate electrode. In the case of constructing the driver circuit for the gate electrode as described above including FIGS. 14 and 16 also, the driver circuit for the source electrode selects data based on a logical state determined by T_R and Q_S after turning on or off a transistor of each pixel commonly connecting to a gate electrode of a certain row, and then determines a voltage for pixel data between each pixel electrode and the common electrode during the period in which the transistor of each pixel in the subsequent row is on. FIG. 24 includes a serial connection of transistors (131) and (132) having T_R and Q_S as respective gate inputs. The source of (131) is connected to data D, and the drain of (132) is connected to the source electrode at the $\{(R-1)\cdot L+S\}^{th}$ row. (133) refers to a capacitor attached to the source electrode. In the configuration shown in FIG. 23, this capacitor is a capacitor for an insulating film, for example, which is provided at the intersection of the source electrode, the gate electrode and the one electrode of the storage capacitor, a capacitor for liquid crystal sandwiched between the source electrode and the common electrode on the opposed substrate and a capacitor provided between the source electrode and the power source electrode as required. The gate electrode potential, V_I and V_C in FIG. 2 and the power source potential are collectively referred by V_{CC} as in FIG. 3. It is assumed here that the driver circuit for the gate electrode commonly connecting to active elements in figures excluding FIG. 24 naturally has a capacitor. Therefore, the capacitor is omitted in the figures. As shown in a timing chart of FIG. 25, T_R refers to a signal of a potential of V_{EE} to V_{GG}. T_R outputs L serial clock pulses from the $\{(R-1)\cdot L+1\}^{th}$ clock pulse from the first clock pulse at V_{GG} (HIGH) of T_1. Q_R refers to a signal of a potential of V_{EE} to V_{GG}. Q_S outputs pulses Q_1 to Q_L one by one in synchronization with the L clock pulses of T_R. The pulse width is substantially the same as a cycle of one pair of clocks at HIGH and LOW in the L serial clock pulses of T_R. When T_R and Q_S are both at V_{GG} (HIGH), that is, the AND is at HIGH, (131) and (132) are turned on and a potential of D is selected so as to be stored in the capacitor (133). When either one of T_R and

Q_S is at V_{EE} (LOW), either one of (131) and (132) is turned off, and (133) dynamically holds the selected potential among the potentials of the source electrode. As the driver circuit for the gate electrode sequentially outputs signals of $P_{R,S}$ to each row, signals of $O_{R,S}$ are sequentially fixed for each column and signals of $O_{R,1}$, $O_{R,2}$ to $O_{R,L}$ having potentials of V_a to V_b are output. In order to alternately drive liquid crystal, a potential of the data D is inverted between V_a and V_b with the midpoint of $(V_a+V_b)/2$ or between $(2V_a-V_b)$ and V_a with the midpoint of V_a, thus the signals of $O_{R,1}$, $O_{R,2}$ to $O_{R,L}$ are also inverted. Although a potential of V_{EE} to V_{GG} ($V_{EE}=2(V_a-V_b)$, V_a, $V_b<V_{GG}$) of the signals T_R and Q_S of the driver circuit for the source electrode can be selected so as to be different from the potential of the signals T_R and Q_s or the like of the driver circuit for the gate electrode, it may be set equal or in the range of a potential of V_{SS} to V_{DD} of the signal $P_{R,S}$. The potential of D is selected at a timing in which the AND of T_R and Q_S becomes HIGH, therefore, a HIGH period of Q_S before the period in which the AND of the Q_S and T_R is at HIGH in the timing chart can be longer than the half cycle of the L serial clocks of T_R as shown in the figure.

(28)

Although the driver circuits for each electrode (128) and (130) of the liquid crystal display shown in FIG. 23 are supplied with input signals of T_R and Q_S or the like and a power source potential from the lead electrodes at the end side of the substrate, it is also possible as shown in FIG. 6 to implement an integrated circuit for supplying these signals and potentials on the substrate in order to further reduce the number of the lead electrodes. FIG. 26 shows a partial plan view of the improved liquid crystal display of FIG. 23. (128) and (130) refer to the driver circuits for gate electrodes and source electrodes as in FIG. 23. (128) and (130) are integrated on a substrate (134) corresponding to (120). (135) refers to an opposed substrate forming a common electrode and corresponds to (121). (135) is attached to (134) in the region excluding the upper left side with reference to a line G-H"-H in which an integrated circuit (145) for supplying signals of T_R, Q_S or the like and a power source potentials to each of (128) and (130) is implemented. (136) refers to a lead electrode which is input with a clock on which the signals such of T_R and Q_S or the like to (128) are based. (137), (138), (139) and (140) refer to lead electrodes which are input with power source potentials denoted by V_{GG}, V_{EE}, V_{DD} and V_{SS} respectively, that is the potentials that HIGH and LOW of signals are based on. Similarly, (141)

refers to a lead electrode which supplies data D to (130), (142) refers to a lead electrode which supplies clocks that signals T_R, Q_S or the like to (130) are based on, and (143) and (144) refer to lead electrodes which supply positive and negative power source potentials denoted by V_{GG} and V_{EE}. Each electrode of (136) to (140) and (142) to (144) are connected to (145). It is needless to mention that (141) can be connected to (145) so that (145) constitutes data to supply to (130). (145) supplies a potential of one electrode of a storage capacitor for pixel data denoted by dashed lines in FIG. 23 input from (128). (125) in FIG. 23 may be connected to an electrode denoted by dashed lines so that the potential of (125) is equal to that of the common electrode on the opposed substrate.

(29)

FIG. 27 is diagrams of driver circuits for source electrodes commonly connecting to active elements of the image display apparatus according to another embodiment of the invention. In the timing chart in FIG. 25, $Q_{R,1}$, $Q_{R,2}$ to $Q_{R,L}$ are sequentially fixed by potentials of data D selected for each cycle of one pair of clocks at HIGH and LOW among L serial clock pulses of T_R. On the other hand, in a timing chart in FIG. 28, $O^J_{R1,1}$, $O^J_{R2,1}$ to $O^J_{R1,L}$, $O_{R2,L}$ (where J=1, 2, 3) are sequentially fixed by potentials of data D_J selected for each half cycle of one pair of clocks at HIGH and LOW among L serial clock pulses of T_{R1} and T_{R2} each of which is at HIGH alternately during the period in which Q_S is at HIGH. By providing three data lines, data of D_1, D_2 and D_3 are supplied in parallel, and Q_S and T_{R1} or T_{R2} determine three signals of $O^1_{R1,S}$, $O^2_{R1,S}$ and $O^3_{R1,S}$ or $O^1_{R2,S}$, $O^2_{R2,S}$ and $O^3_{R2,S}$ at the same timing. The basic configuration of the circuit in FIG. 27 is the same as of FIG. 24, and it includes a serial connection of two transistors. (146) and (147) having T_{R1} and Q_S as the common gate inputs select $O^1_{R1,S}$, (148) and (149) having T_{R1} and Q_S as the common gate inputs select $O^2_{R1,S}$ and (150) and (151) having T_{R1} and Q_S as the common gate inputs select $O^3_{R1,S}$ from D_1, D_2 and D_3 respectively. Meanwhile, (152) and (153) having T_{R2} and Q_S as the common gate inputs select $O^1_{R2,S}$, (154) and (155) having T_{R2} and Q_S as the common gate inputs select $O^2_{R2,S}$ and (156) and (157) having T_{R2} and Q_S as the common gate inputs select $O^3_{R2,S}$ from D_1, D_2 and D_3 respectively. The selection is carried out when each of T_{R1} and Q_S or T_{R2} and Q_S is at V_{GG} (HIGH), that is, the AND is at HIGH. When either one is at V_{EE} (LOW), that is, the AND is at LOW, the selected potentials are held. It is assumed here that D_1, D_2 and D_3 are data corresponding to each color signal of R (red), G (green) and B (Blue)

which is selected according to the position of color filters in the column direction in pixels of the selected row of the liquid crystal display. For example, when color filters in the column direction is in the order of G, B, R, G, B, R and ..., D_1 corresponds to G, D_2 corresponds to B and D_3 corresponds to R. Accordingly, Q_S and T_{R1} or T_{R2} select three columns at the same time, thus each source electrode potential for G, B and R is determined. When the color filters in the pixels of the selected row are in the order of B, R and G, D_1, D_2 and D_3 each correspond to data of the same color of B, R and G according to the selection of the row. In FIGS. 27 and 28, potentials of adjacent three columns are simultaneously determined by Q_S and T_{R1} or T_{R2}. However, as in FIG. 6 in which the integrated circuits (51) to (54) transmit signals to each of the four groups of the source electrodes of the liquid crystal display, the source electrodes of the liquid crystal display in FIG. 23 are divided into three groups, and D_1, D_2 and D_3 are assumed to be data for determining a potential of the source electrode of each group. By arranging the circuit such that a potential of each source electrode is determined by selecting data based on a logical state determined by two inputs of Q_S and T_{R1} or Q_S and T_{R2} for each group, source electrode potentials in one column for each of the three groups are simultaneously deremined. By arranging M (where M>3) data lines to supply data of D_1, D_2, D_3 to D_M in parallel, potentials of the source electrodes at M columns can be fixed simultaneously. Further, since input signals of T_{R1} and T_{R2} are K signals respectively, input signals of Q_S are L signals and input signals of D_J are M signals, potentials of the source electrodes at 2K·L·M columns are determined by (2K+L+M) signals.

(30)

FIG. 29 shows a diagram of a driver circuit for the source electrode commonly connecting to active elements like FIG. 24, which includes a transistor (158) having Q_S as a gate input and T'_R as a source potential and a transistor (160) having a drain output of (158) as a gate input and connecting the data D to the source. (159) refers to a capacitor provided between the drain of (158) and the power source potential V_{SS} so as to hold the drain potential $P_{R,S}$ dynamically. The output $O_{R,S}$ of (160) corresponds to a potential of the source electrode at the $\{(R-1)\cdot L+1\}^{th}$ column. The circuit for outputting $P_{R,S}$ has the same configuration as that of FIG. 14. As shown in the timing chart in FIG. 15, when the AND of T'_R and Q_S is at HIGH, $P_{R,S}$ is at V_{DD} and turns on (160), thereby leading a potential of D to $Q'_{R,S}$. Subsequently, when T'_R is at

LOW and Q_S is at HIGH, $P_{R,S}$ is at V_{SS} and turns off (168), thereby holding a potential of $O_{R,S}$ dynamically. When a potential of D is inverted between V_a and V_b or between $(2V_a-V_b)$ and V_b with the midpoint of V_a as shown in FIG. 25, a power source potential can be fixed at $V_{EE}=V_{SS}=(2V_a-V_b), V_a, V_b<V_{DD}<V_{GG}$. The circuit for outputting the gate signal $P_{R,S}$ may be constructed as in FIGS. 3, 7, 8, 10 and 16.

(31)

FIG. 30 is a diagram of driver circuits for source electrodes commonly connecting to active elements like FIG. 27. FIG. 30 includes a serial connection of a transistor (161) having V_{SS} as a source potential and having ϕ as a gate input and a transistor (162) having Q's as a drain potential and having T_{R1} as a gate input. (163), (164) and (165) refer to transistors having an output $P_{R1,S}$ obtained by the serial connection of the transistors (161) and (162) as a common gate input and connecting data D_1, D_2 and D_3 to the respective sources. FIG. 30 further includes a serial connection of a transistor (166) having V_{SS} as a source potential and ϕ_2 as a gate input and a transistor (167) having Q's as a drain potential and T_{R2} as a gate input. (168), (169) and (170) refer to transistors having an output $P_{R2,S}$ obtained by the serial connection of the transistors (166) and (167) as a common gate input and connecting the data D_1, D_2 and D_3 to the respective sources. Each output of $O^1_{R1,S}$, $O^2_{R1,S}$ and $O^3_{R1,S}$ or $O^1_{R2,S}$, $O^2_{R2,S}$ and $O^3_{R2,S}$ is fixed at a same timing of T_{R1} or T_{R2}, thereby determining a potential of the source electrode. The circuits outputting $P_{R1,S}$ and $P_{R2,S}$ have the same configuration as that of FIG. 8. In substantially the same manner as that of the timing chart in FIG. 17 of the similar circuit configuration of FIG. 16, $P_{R1,S}$ and $P_{R2,S}$ are at V_{DD} when the AND of Q_S and T_{R1} or T_{R2} is at HIGH. The transistors commonly connecting the output of $P_{R1,S}$ and $P_{R2,S}$ to the gates are turned on and a potential of D_J is led to $O^J_{R1,S}$ and $O^J_{R2,S}$ (J = 1, 2, 3). When the AND of Q_S and T_{R1} or T_{R2} is at LOW, the transistors having clocks ϕ_1 or ϕ_2 as gate inputs are at the potential of V_{SS} to be pre-charged. Thus, the transistors commonly connecting the output of $P_{R1,S}$ and $P_{R2,S}$ to the gates are turned off and potentials of $O^J_{R1,S}$ and $O^J_{R2,S}$ are held dynamically.

(32)

The driver circuits for these source electrodes select a potential of data D_J when the AND of T_R and Q_S or the like is at HIGH, and dynamically holds the potential when the AND thereof is at LOW in order to determine signals for source electrode columns. At this time,

each transistor connecting to each pixel electrode of pixels in one row are turned on to transmit signals of the source electrodes to the pixel electrodes. Then, each of the transistors is turned off to hold the potentials of the pixel electrodes. The driver circuits for the source electrodes can be constructed such that a static signal is fixed at the source electrode while the pixel data is determined between the pixel electrode and the common electrode. FIG. 31 shows a diagram of such driver circuit for source electrodes, which is constructed by combining the circuits shown in FIGS. 24 and 3. That is, the circuit includes a serial connection of transistors (171) and (172) having T_R and Q_S as respective gate inputs. The source of (171) is connected to data D_J and the drain of (172) is connected to each gate of transistors (174) and (176) and a capacitor (173). Each source of (174) and (176) and one electrode of (173) are connected to a power source V_X. The drain of (174) is connected in series to the gate of a transistor (177) which is connected in series to a signal ψ through a capacitor (175) and to the transistor (176). The drain of (177) is connected to a power source V_Y. (171) and (172) are turned on when the AND of T_R and Q_S is at HIGH and selects a potential of D_J as in FIG. 25, and then store the potential in a capacitor (173) and capacitors between each gate and source of (174) and (176). Meanwhile when the AND thereof is at LOW, (171) and (172) are turned off and the potential of $O^J_{R,S}$ of the capacitors is held. As shown in a timing chart in FIG. 32, (174) and (146) are turned off when the a potential of D_J which is selected when the AND of T_R and Q_1 is at HIGH, that is $O^J_{R,1}$ is at V_U (LOW), and (174) and (176) are turned on when $O^J_{R,1}$ is at V_W (HIGH), thus the output $Z^J_{R,1}$ is at V_X (LOW). The transistor (178) connecting V_X to the source, connecting the gate of (177) to the drain and having a signal θ as a gate input fixes a potential of the gate of (177) and of the capacitor (175) at V_X when θ is at V_{GG} (HIGH) and ψ is at V_{EE} (LOW) in the scan period for pixels in one row. When (174) and (176) are off and f is at V_{GG} (HIGH), (177) has a gate potential at HIGH and thus is turned on. Then, $Z^J_{R,1}$ is at HIGH. A period in which the driver circuits for the gate electrodes turn on transistors in the pixels in one row where $P_{R,S}$ and V_{DD} generated at a logical state determined by T_R and Q_S or the like is at HIGH is included in the period in which ψ is at HIGH, which means pixel data is determined by a static potential of the source electrode. (V_X, V_Y) are fixed at the potentials (V_a, V_b) or ($2V_a$-V_b, V_a) of the data in the timing charts in FIGS. 25 and 28, and selected among $V_{EE}=V_{SS}=V_U=V_X$ and $V_Y=V_W=V_{DD}=V_{GG}$. The circuit outputting the gate signal $O^J_{R,S}$ of (174) and (178) may be constructed as in FIGS. 29

and 30. The gate signal of (178) may be either T_R or Q_S.

(33)

FIG. 33 is a diagram of a driver circuit for source electrodes like FIG. 31. (179), (180), (181), (182), (183), (184) and (185) correspond to (171), (172), (173), (174), (175), (176) and (177) respectively. As shown in a waveform of D_J in the timing chart in FIG. 32, when constructing the circuit for obtaining desired data such that V_W (HIGH) is selected in the former half period and either V_U (LOW) or V_W (HIGH) is selected in the latter half period while T_R and Q_S are both at HIGH, (179) and (180), which are turned on when the AND of T_R and Q_S is at HIGH, turn on (182) and (184), thereby fixing a potential of the gate of (185) and of the capacitor (183) at V_X in the former period, and determines the desired selected data as $O^J_{R,S}$ in the latter half period. Therefore, the function of (178) in FIG. 31 can be included in (182).

(34)

In FIG. 31, the potential of D_J is selected based on a logical state determined by two inputs T_R and Q_S to determine the potential of $D^J_{R,S}$. However, it is also possible to construct the circuit such that $Z_{R,S}$ is output to source electrode columns when $O_{R,S}$ is determined by selecting the power source potential of V_W at a logical state determined by two inputs of data D_R and Q_S having a potential of V_{EE} to V_{GG}. D_R in this case corresponds to T_R which has been described heretofore. While T_R is outputting L serial clock pulses, Q_S sequentially outputs data of V_{EE} (LOW) and V_{GG} (HIGH) so as to overlap with the whole HIGH period. Meanwhile, when T_R is at LOW and outputs no clock pulse, Q_S sequentially outputs LOW pulses in the similar manner. FIG. 34 is a driver circuit for source electrodes which selects a potential of V_W based on a logical state determined by two inputs D_R and Q_S and determines a potential of $O_{R,S}$ in order to transmit static potentials to source electrode columns while f is at HIGH. (186), (187), (188), (189), (190), (191), (192) and (193) correspond to (171), (172), (173), (174), (175), (176), (177) and (178) in FIG. 31 respectively. The source of (186) is at a power source potential V_W and (187) has data D_R as a gate input. FIG. 35 is a timing chart of the circuit in FIG. 34. When Q_S is at HIGH and D_R is at HIGH, (186) and (187) are turned on, and $O_{R,S}$ is at V_W (HIGH). When Q_S is at HIGH while D_R is at LOW, (187) is off. Therefore, $O_{R,S}$ holds an initially fixed potential at LOW, and (186) is turned off when Q_S is at LOW, which means $O_{R,S}$ is maintained at a previous potential. (194) is turned on by a gate signal θ which is at V_{GG}

(HIGH) before V_W is selected by D_R and Q_S when ψ is at V_{EE} (LOW) within a scanning period for pixels in one row, and initially fixes the potential of $O_{R,S}$ at V_X. At the same time, a potential of the gate of (192) and of the capacitor (190) is fixed at V_X by (193). When selection of V_W by D_R and Q_S is complete, f is at V_{GG} (HIGH). When $O_{R,S}$ is at LOW, $Z_{R,S}$ is maintained at V_Y (HIGH). When $O_{R,S}$ is at HIGH, $Z_{R,S}$ is maintained at V_X (LOW). During the period indicated by $P_{R,S}$ in which pixels in one row are turned on, ψ is in the HIGH period as in FIG. 32. In this circuit, a gate signal of (193) may be Q_S, a gate signal of (186) may be data D_S and a gate signal of (187) may be T_R. In that case, D_S corresponds to Q_S, and T_R may output data of V_{EE} (LOW) and V_{GG} (HIGH) when Q_S is at HIGH so as to overlap with the HIGH period, and likewise to be at LOW when Q_S is at LOW. The gate signal of (193) at this time may be connected to T_R. The circuit including (186), (187), (188) and (184) can be used as a driver circuit which holds a potential of $O_{R,S}$ dynamically and fixes a signal for a source electrode column.

(35)

FIG. 36 is a driver circuit for source electrodes, including data D_J, invert data of D_J, and a pair of the circuits in FIG. 24. FIG. 36 fixes $O^J_{R,S}$ and the invert signal of $O^J_{R,S}$ by selecting the potentials of D_J and the invert data of D_J based on a logical state determined by T_R and Q_S, and statically outputs $Z^J_{R,S}$ by controlling the gate of a transistor connecting V_X (LOW) to the source and V_Y (HIGH) to the drain. FIG. 36 includes a serial connection of a transistor (195) and a transistor (196) having T_R and Q_S as the gate inputs. The source of (195) is connected to D_J and the drain of (196) is connected to a capacitor (197) connecting V_X to one electrode thereof and the gate of a transistor (201) connecting V_X to the source. Similarly, FIG. 36 includes a serial connection of a transistor (198) and a transistor (199) having T_R and Q_S as the gate inputs. The source of (198) is connected to the invert data of D_J and the drain of (199) is connected to a capacitor (200) connecting V_Y to one electrode thereof and the gate of a transistor (202) connecting V_Y to the drain. (201) and (202) are connected in series. When the AND of T_R and Q_S is at HIGH, (195), (196), (198) and (199) are turned on, and select potentials of D_J and the invert data of D_J at V_U (LOW) and V_W (HIGH) to store them in the capacitors (197) and (200). When the AND of T_R and Q_S is at LOW, the transistors (195), (196), (198) and (199) are turned off to hold each potential of $O^J_{R,S}$ and the invert output of $O^J_{R,S}$ of the capacitors. When

($O^J_{R,S}$, the invert output of $O^J_{R,S}$) is (V_U, V_W), (201) is turned off while (202) is turned on, which causes $Z^J_{R,S}$ to be at V_Y (HIGH). Meanwhile, when ($O^J_{R,S}$, the invert output of $O^J_{R,S}$) is (V_W, V_U), (202) is turned off while (201) is turned on, which causes $Z^J_{R,S}$ to be at V_X (LOW), thus the potential of the source electrode column is statically fixed. The capacitors (197) and (200) can be formed by a capacitance between the gate and source of (201) and a capacitance between the gate and drain of (202). Each one electrode of the capacitors connecting to V_X and V_Y can be connected to V_Y and V_X.

(36)

The driver circuit for the source electrodes as described above according to an embodiment is driven by providing M data lines. However, it is also possible to divide gate electrodes of a liquid crystal display into M groups and separate power source lines to supply potentials for turning on transistors connecting to pixel electrodes into each group. In this case, V_1 to V_M are potentials of the power osurce line for each group, a circuit for transmitting a signal to the gate electrode by selecting a potential based on a logical state determined by two inputs T_R (where R=1, 2 to K) and Q_S (where S=1, 2 to L) is disposed in each group, and T_R and Q_S are used as common signals for each group. Thus, potentials of the gate electrodes at K·L·M rows can be determioned.

(37)

FIG. 37 is a diagram of a driver circuit for the gate electrode commonly connecting to active elements of the image display apparatus according to another embodiment of the invention. FIG. 38 is a timing chart showing an operation thereof. FIG. 37 includes a serial connection of transistors (203), (204) and (205) having ϕ, T_R and Q_S as respective gate inputs. The source of (203) is connected to a power source V_{SS} which turns off a transistor connecting to a pixel electrode and is commonly supplied to a circuit in each row. The drain of (205) is connected to a power source potential V_J (where J=1 to M) which is independently supplied to each group. A connection point of the drain of (203) and the source of (204) transmits a signal $P^J_{R,S}$ to a {(J - 1)·K·L+(R-1)·L+S}th row. V_J is a power source potential which is at V_{DD} while sequentially outputting signals which turn on transistors to K·L rows from the {(J-1)·K·L+1}th row, while it is at V_{SS} in other periods. When T_R and Q_S are both at V_{GG} (HIGH), (204) and (205) are turned on. When V_J is t V_{DD}, $P^J_{R,S}$ is at VDD (HIGH). When V_J is at V_{SS}, V_{SS} is at LOW. When

the AND of T_R and Q_S is at LOW, $P^J_{R,S}$ has a potential of V_{SS} (LOW) to be pre-charged through (203) which is turned on when ϕ is at V_{GG} (HIGH). $P^1_{R,1}$ is a signal at a $\{(R-1)\cdot L+1\}^{th}$ row. $P^2_{R,1}$ is a signal at a $\{K\cdot L+(R-1)\cdot L+1\}^{th}$ row which is at HIGH when a potential of V_2 is selected after a HIGH signal of $P^1_{R,1}$ is transmitted and signals of T_R and Q_1 have made a circuit and thus the AND of T_R and Q_1 becomes HIGH again.

(38)

FIG. 39 is a diagram of the driver circuit for the gate electrode shown in FIG. 3. As in FIG. 37, a power source V_{DD} is disposed as V_J in each group, and signals T_R and Q_S are commonly supplied to each group, thereby transmitting signals to gate electrodes at K·L·M rows. (208), (207), (206) and (209) correspond to (17), (18), (19) and (20) respectively. Gate signals of (206) and (208) are connected to Q_S. An input signal to a capacitor (207) is connected to T_R. The source of (208) is connected to the power source V_{SS} which is commonly supplied to the circuit in each row of FIG. 39 type. The drain of (209) is connected to V_J. A connection point of the drain of (208) and the source of (209) transmits a signal $P^J_{R,S}$. The circuit shown in FIG. 12 can be constructed in the similar manner as the above by disposing the power sources V_{DD} and V_{BB} in each group as V^J_{DD} and V^J_{BB} respectively. Alternatively, by connecting the drain of (205) shown in the circuit in FIG. 37 to Q'_S of same phase as Q_S at a potential of V_{EE} to V_{GG}, and fixing a gate signal of (205) at a signal having the same phase as V_J at a potential of V_{SS} to V_{DD}, thereby turning off (205) when the signal having the same phase as V_J is at V_{EE} (LOW) while turning on (205) when the signal having the same phase as V_J is at V_{GG} (HIGH), the similar output of $P^J_{R,S}$ to that in FIG. 38 can be obtained. In the circuit, the source of (203) can be connected to Q'_S or T_R if the LOW potential of T_R is at V_{SS}. Similarly, by connecting the drain of (205) shown in the circuit in FIG. 37 to T'_R of the same phase as T_R at a potential of V_{SS} to V_{DD}, and fixing a gate signal of (204) at a signal having the same phase as V_J at a potential of V_{EE} to V_{GG}, thereby turning off (204) when the signal is at V_{EE} (LOW) while turning on (204) when it is at V_{GG} (HIGH), the signal of $P^J_{R,S}$ can be output. The source of (203) can be connected to T'_R or Q_S as well if the LOW potential of Q_S is at V_{SS}. Such a circuit corresponds to the one in which a control function enabling the individual operation for each group is added to the circuit transmitting signals which turns on or off transistors to a gate electrode commonly connecting to the transistors by selecting a potential based on a logical state determined by two

inputs T_R and Q'_S or T'_R and Q_S. In this case, the control signal which is added with another input besides the two inputs of T_R and Q_S corresponds to the above-described signal having the same phase as V_J at a potential of V_{EE} to V_{GG}. When the signal is at V_{GG}, an on or off signal is transmitted while when the signal is at V_{EE}, transistors are held off. It is needless to mention that the same function can be obtained by connecting (203), (204) and (205) in FIG. 37 or (209) in FIG. 39 in series to a transistor having a control signal of the same phase as V_J at a potential of V_{EE} to V_{GG} as an gate input, and replacing V_J by V_{DD} to connect to the drains. The power source potentials classified heretofore as V_{SS} and V_{DD} as V_{EE} and V_{GG} can be set as $V_{EE}=V_{SS}$ or $V_{GG}=V_{DD}$ as needed to operate the circuit.

(39)

In a liquid crystal display having diodes as active elements connecting to pixel electrodes, row electrodes connecting to the diodes may be divided into M groups. By adding a control function enabling an individual operation for each group to the driver circuits for row electrodes shown in FIG. 20, a potential can be selected based on a logical state determined by three inputs including an additional input of a control signal V_J or V'_J as well the two inputs T_R and Q_S or T'_R and Q'_S (where R=1, 2 to K, S=1, 2 to L), thus potentials of two lines of row electrodes used in pairs at K·L·M rows can be determined. FIG. 40 show diagrams of driver circuits for row electrodes commonly connecting to active elements of the image display apparatus according to another embodiment of the invention. FIG. 41 is a timing chart showing an operation thereof. V_J and V'_J (where J=1 to M) are control signals for controlling an operation for each group. T_R and Q_S or T'_R and Q'_S are common signals for each group. $P^J_{R,S}$ and $P'^J_{R,S}$ are signals for driving two row electrodes used in pairs in the pixels at a $\{(J-1)\cdot K\cdot L+(R-1)\cdot L+S\}^{th}$ row. $P^J_{R,S}$ and $P'^J_{R,S}$ are transmitted to the row electrodes after selecting V_{DD}, V_{SS} or a potential in the vicinity of V_{SS}, or V_{DD}, V_{HH} or a potential in the vicinity of V_{HH}. In the circuit outputting $P^J_{R,S}$, an N-type semiconductor layer of a diode (210) is connected to T_R while a P-type semiconductor layer thereof is connected to Q_S through a resistor (211). Also, an N-type semiconductor layer of a diode (212) is connected to V_J while a P-type semiconductor layer thereof is connected to the P-type semiconductor layer of (210). Meanwhile in the circuit outputting $P^{J'}_{R,S}$, a P-type semiconductor layer of a diode (213) is connected to T'_R while an N-type semiconductor layer thereof is connected to Q'_S through a

resistor (214). Also, a P-type semiconductor layer of a diode (215) is connected to V'_J while an N-type semiconductor layer thereof is connected to the N-type semiconductor layer of (213). Since T_R and Q_S are signals at V_{SS} to V_{DD}, (212) is biased in the reverse direction when V_J is at V_{DD} (HIGH) and the potential of $P^J{}_{R,S}$ is fixed by the signals of T_R and Q_S. Meanwhile, when V_J is at V_{SS} (LOW), (212) is biased in the forward direction and the potential of $P^J{}_{R,S}$ has V_{SS} or a potential in the vicinity of V_{SS}. Similarly, since T'_R and Q'_S are signals at V_{SS} to V_{HH}, (215) is biased in the reverse direction when V'_J is at V_{DD} (LOW) and the potential of $P^{J'}{}_{R,S}$ is fixed by the potentials of T'_R and Q'_S. When V'_J is at V_{HH} (HIGH), (215) is biased in the forward direction and the potential of $P^{J'}{}_{R,S}$ has V_{HH} or a potential in the vicinity of V_{HH}. During the period in which HIGH or LOW signals are sequentially transmitted to a pair of row electrodes at K·L rows from the $\{(J-1)\cdot K\cdot L \cdot L+1\}^{th}$ row, V_J or V'_J is at V_{DD}(HIGH) or V_{DD}(LOW). An operation by the signals T_R and Q_S or T'_R and Q'_S during this period is similar to that described with reference to FIG. 20. In other periods, V_J or V'_J is at V_{SS}(LOW) or V_{HH}(HIGH), and row signals are at V_{SS} or a potential in the vicinity of V_{SS}, or V_{HH} or a potential in the vicinity of V_{HH}. $P^1{}_{R,1}$ and $P^{1'}{}_{R,1}$ are signals for two row electrodes used in pairs in the pixels at the $\{(R-1)\cdot L+1\}^{th}$ row. $P^2{}_{R,1}$ and $P^{2'}{}_{R,1}$ are signals for two row electrodes used in pairs in the pixels at the $\{K\cdot L+(R-1)\cdot L+1\}^{th}$ row, which are at HIGH and LOW after HIGH and LOW signals of $P^1{}_{R,1}$ and $P^{1'}{}_{R,1}$ are transmitted and signals of T_R and Q_1 or T'_R and Q'_1 have made a circuit and thus the respective AND of T_R and Q'_1, and of T'_R and Q'_1 is at a previous state again. As described in FIG. 20, the signals T_R and Q_S connecting to (210) and (211) or the signals T'_R and Q'_S connecting to (213) and (214) can be exchanged as Q_S and T_R or Q'_S and T'_R respectively. Similarly, the signals V_J and Q_S connecting to (212) and (211) or the signals V'_J and Q'_S connecting to (213) and (214) can be exchanged as Q_S and V_J or Q'_S and V'_J respectively. In that case, V_J and V'_J correspond to the power source lines for supplying potentials to row electrodes, and V_1, V'_1, V_2, V'_2 to V_H and V'_H each correspond to the potentials of a power source line in each group when the row electrodes of the liquid crystal display are divided into M groups. When V_J is at V_{DD}(HIGH) and T_R and Q_S are both at V_{DD} (HIGH), that is the AND is at HIGH, $P^J{}_{R,S}$ is at V_{DD} (HIGH). When V_J is at V_{DD}(HIGH) and the AND of T_R and Q_S is at LOW, $P^J{}_{R,S}$ is in the vicinity of V_{SS} (LOW). When V'_J is at V_{DD}(LOW) and T'_R and Q'_S are both at V_{DD} (LOW), that is, the OR is at LOW, $P^{J'}{}_{R,S}$ is at V_{DD} (LOW). When V'_J is at V_{DD}

(LOW) and the OR of T'_R and Q'_S is at HIGH, $P^{J'}_{R,S}$ is in the vicinity of V_{HH} (HIGH). When V_J and V'_J are at V_{SS} (LOW) and V_{HH} (HIGH) respectively, $P^J_{R,S}$ and $P^{J'}_{R,S}$ are at V_{SS} (LOW) and V_{HH} (HIGH), which are independent of T_R, Q_S, T'_R and Q'_S, thus the similar operation as that in FIG. 41 is obtained.

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By individually disposing V_1, V'_1, V_2, V'_2 to V_H and V'_H in each driver circuit for the row electrode in the pixels at adjacent M rows having T_R and Q_S or T_R' and Q'_S as the common inputs, the power source potentials and the control signals V_J and V'_J described with reference to FIGS. 37 to 41 can determine pixel data for the K·L rows by one drive in the vertical selective direction in the pixels in the liquid crystal display shown in FIGS. 1, 6, 18 and 23. Thus, pixel data for all the pixels at the K·L·M rows can be determined by M drives.

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[Effect]

As described above, the invention reduces a load of a connection between lead electrodes on a substrate of a liquid crystal display and off-substrate driver circuits which has been a problem in a high-density image display apparatus, by producing a driver circuit for electrodes commonly connecting to active elements at a step of forming a substrate of a liquid crystal display included in an active matrix image display apparatus in which liquid crystal is driven by active elements in each pixel electrode, thereby integrating the circuit on the same substrate. The driver circuit simply selects a potential at a logical state determined by two inputs or three inputs, thus is effective in manufacturing. The driver circuit having transistors as active elements are constructed to consume few direct current. The driver circuit having diodes as active elements are constructed such that direct current consumption is equal to or less than one-severalth of that in the signal lines T_R, Q_S or the power source line V_J. Thus, the invention can be suitably applied to an image display apparatus.

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4. [Brief Description of the Drawings]

FIG. 1 is a plan view of a liquid crystal display of an image display apparatus of the invention. FIG. 2 is a configuration diagram of a pixel. FIG. 3 is a diagram of driver circuits for gate electrodes commonly connecting to active elements. FIG. 4 is a timing chart showing

an operation of the circuit in FIG. 3. FIG. 5 is a substrate section diagram showing that the circuit in FIG. 3 is integrated on a substrate having a pixel electrode connecting to an active element. FIG. 6 is a plan view of a liquid crystal display of the image display apparatus of the invention. FIGS. 7 and 8 are diagrams of driver circuits for gate electrodes commonly connecting to active elements. FIG. 9 is a timing chart showing an operation of the circuits in FIGS. 7 and 8. FIGS. 10, 11 and 12 are diagrams of driver circuits for gate electrodes commonly connecting to active elements. FIG. 13 is a timing chart showing an operation of the circuit in FIG. 12.

FIGS. 14 and 16 are diagrams showing driver circuits for gate electrodes commonly connecting to active elements. FIGS. 15 and 17 are timing charts showing operations of the circuits in FIGS. 14 and 16 respectively.

FIG. 18 is a plan view of a liquid crystal display of an image display apparatus according to an embodiment of the invention. FIG. 19 is a configuration diagram of a pixel. FIG. 20 is diagrams of driver circuits for row electrodes commonly connecting to active elements. FIG. 21 is a timing chart showing an operation of the circuit in FIG. 20. FIG. 22 is a substrate section diagram showing that the circuit in FIG. 20 is integrated on a substrate having a pixel electrode connecting to an active element.

FIG. 23 is a plan view of a liquid crystal display of the image display apparatus according to an embodiment of the invention. FIG. 24 is a diagram of a driver circuit for source electrodes commonly connecting to active elements. FIG. 25 is a timing chart showing an operation of the circuit in FIG. 24. FIG. 26 is a partial plan view of the improved liquid crystal display of FIG. 23.

FIGS. 27, 29 and 30 are diagrams of driver circuits for source electrodes commonly connecting to active elements. FIG. 28 is a timing chart showing an operation of the circuit in FIG. 27.

FIGS. 31, 33, 34 and 36 are diagrams of driver circuits for source electrodes commonly connecting to active elements. FIGS. 32 and 35 are timing charts showing operations of the circuits in FIGS. 31 and 34 respectively.

FIG. 37 is a diagram of a driver circuit for gate electrodes commonly connecting to active elements of the image display apparatus according to another embodiment of the invention.

FIG. 38 is a timing chart showing an operation of the circuit in FIG. 37. FIG. 39 is a diagram of a driver circuit for gate electrodes commonly connecting to active elements.

FIG. 40 is diagrams of driver circuits for row electrodes commonly connecting to active elements of the improved image display apparatus according to another embodiment of the invention. FIG. 41 is a timing chart showing an operation of the circuit in FIG. 40.

(1) : a substrate having multiple pixel electrodes connecting to active elements

(2) : an opposed substrate having common electrodes

(3) : a pixel electrode

(4) : a source electrode

(5) : a gate electrode

(6) : an electrode connecting to the common electrode

(7) : an electrode commonly connecting to one electrode of a storage capacitor for pixel data.

(8) : electrodes for signals and power input to a driver circuit for gate electrodes commonly connecting to the active elements

(9) : a driver circuit for gate electrodes commonly connecting to the active elements integrated on (1)